QPVP31 VersaPHY™ - 2 Serial Port and 16 GPIO

Features:

- **IEEE-1394-2008 Beta compatible PHY/Link Interface**
  - **Connects to IEEE-1394b PHY devices**
- **Supports 2 Serial Port profiles**
- **Supports 16 programmable GPIOs**
- **Settable VP-Label**
  - **Locally and over the bus**
- **Alleviates the need for polling through unsolicited response support**
- **High resolution time stamp for each input change event**
- **Low Latency GPIO**
  - **Can detect 40ns input transitions**
  - **Maximum continuous input change support is 750kHz across all inputs (12Mb/s)**
- **Supports serial baud rate up to 256kb/s**
- **Virtual COM port and GPIO support for:**
  - **Windows XP and Vista**
- **Virtual COM port makes 1394 transparent to host application and device**

The QPVP31 connects two of the most common interfaces, serial port and general purpose I/O, to the high performance serial bus IEEE-1394-2008 [also known as FireWire]. The QPVP31 implements VersaPHY™[1] Technology which enables these relatively slow interfaces to share in the abundant bandwidth capabilities of 1394 with no device software. The QPVP31 connects to the 1394 beta PHY layer using the IEEE-1394-2008 defined PHY/Link interface and support data rates of S100 (98.304Mb/s), S200 (196.608Mb/s), S400 (393.216Mb/s) and S800 (786.432Mb/s). Each device function (Serial Ports A and B, and GPIO) has its own profile registers and are independently addressable through VersaPHY static VP-Labels. IEEE-1394 Physcial-IDs maybe used for device discovery.

Serial Ports

The QPVP31 provides two universal asynchronous receiver and transmitter (UART) ports. Each port's receiver and transmitter can store up to 16 bytes in their respective FIFOs. The UART configures and communicates with 8 bits of data, parity none, stop bit 1 and no flow control. It supports baud rates from 300 to 256kb/s. The two UARTS are represented individually through their own VersaPHY profile registers.

GPIO

The QPVP31 provides 16-channel, 40ns bidirectional digital general purpose I/Os. Easily fast enough for pulse-width modulation (PWM) or digital communication. The I/Os maybe configured as input or output. Each channel is compatible with 5V/TTL, sinking/sourcing signals. Additionally, VersaPHY time stamping may be enabled. This allows a 1394 bus synchronized 20ns resolution timestamp packet to be sent along with an unsolicited response every time an input changes state. The synchronous time stamp allows multiple processes to be correlated when processing data.

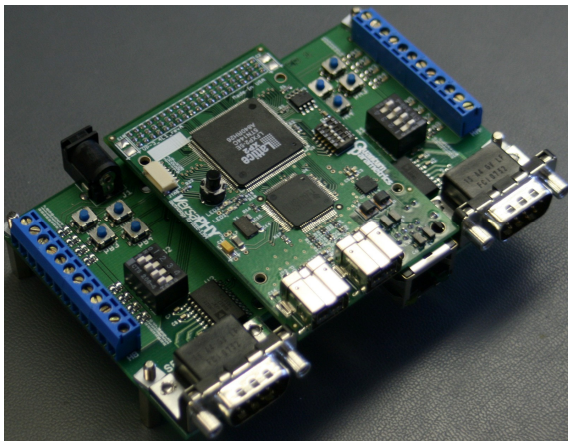
PHY/Link Interface

The QPVP31 provides an IEEE-1394-2008 Beta parallel PHY/Link interface. The Beta PHY/Link interface provides mechanisms to support communication between a discrete PHY and the QPVP31 at speeds of S100, S200, S400, and S800 with a data path that is 8-bits wide.

Development Kit

QP provides evaluation platforms for our VersaPHY devices. The QPVP31 development platform consists of a VersaPHY interface board (two bilingual ports and one UTP long haul port) and a two serial ports and 16 GPIO board.

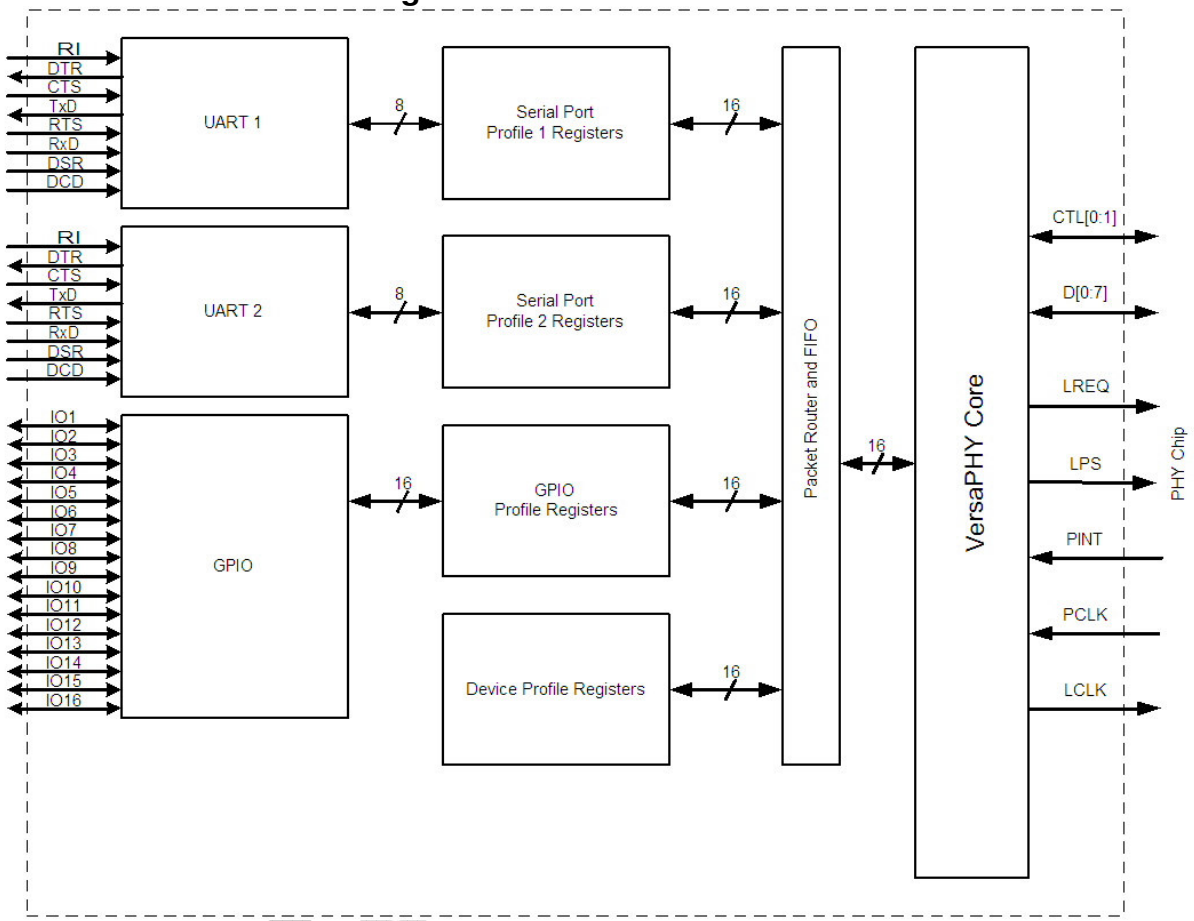
[1] **VersaPHY is a trademark of Quantum Parametrics LLC**



QPVP31 Development Platform

Included with the development kit is the VersaPHY Framework (VP-Framework™) software developer kit. VP-Framework, like VersaPHY itself, supports very simple applications only wanting to have register access through a full VersaPHY controller implementations. Currently the VP-Framework is only available for Windows XP and Vista.

QPVP31 Functional Block Diagram



Application Information